25 Spring ECEN 720: High-Speed Links: Circuits and Systems Pre-lab Report

Lab4: Receiver Circuits

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| Range (±σ) | Coverage Probability | Yield Rate (%) |
| ±1σ | 68.27% | 68.27% |
| ±2σ | 95.45% | 95.45% |
| ±3σ | 99.73% | 99.73% |
| ±4σ | 99.93% | 99.93% |

* If a circuit design allows ±3σ variation, the yield rate is approximately 99.73%, meaning **around 27 out of 10,000 units might be out of spec**.
* If the design tolerates ±4σ, the yield increases to 99.9937%, ensuring almost all products meet specifications.

2. A receiver is characterized by its input sensitivity which represents the voltage resolution, and by the set-up and hold times (tS and tH) which represent the timing resolution as illustrated with the light rectangle in Figure 1. The center of the dark rectangle is shifted by the offset time and offset voltage from the center of the light rectangle. Input sensitivity consists of input voltage offset, input referred noise, and minimum latch resolution voltage. A Strong-Arm latch input static voltage offset is 10mV, minimum latch resolution from hysteresis is bounded to 2mV, and 2mV sigma of input referred noise. The aperture time and the combined set-up and hold time (tS+tH) of the latch are 10ps and 20ps, respectively. Also assume that the receiver sampling clock has a 10ps timing offset and 1ps sigma of random jitter. The target BER is 10-12 (Hint: how many standard deviations does this imply?)

On the 6Gb/s NRZ eye diagram obtained in Lab 2 over B12 backplane channel (either from MATLAB or CADENCE), draw the window that the incoming signal needs to avoid such that the receiver will reliably translate the voltage waveform received from the channel into logic 1’s or 0’s under worst-case combinations of offsets and resolution.

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3. Demultiplexer (DeMUX) is often used to deserialize a stream of high speed data. It can be implemented after the receiver circuit to generate lower speed data. Please design a 1:4 binary-tree DeMUX that deserializes 6Gb/s data into 1.5Gb/s data. Figure 9 is an example of 1:2 De-MUX, please refer to [3] as a reference. You may use behavioral models to implement the building blocks in the DeMUX. Plot the simulation results that verify the operation of DeMUX.

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| Using 3G for first stage decoding, and 1.5G for second stage decoding |
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|  |

* Appendix

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